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IN THE CLAIMS:

Please cancel claims 1-10 and 19-27 without prejudice or disclaimer. All pending claims and their present status are produced below.

1-10. (Cancelled)

11. (Previously Presented) An embedded processor for providing connectivity in a communications system, comprising:

a 32-bit arithmetic-logic unit (ALU) comprising a first input, a second input, and an output, the ALU for performing an operation on a first 32-bit operand and a second 32-bit operand and for producing a 32-bit result, the operation specified in a 32-bit instruction fetched by the ALU;

a 32-bit register file for temporarily holding data, the 32-bit register file coupled to the first input of the ALU and communicatively coupled to the second input of the ALU for providing the first and the second 32-bit operand and coupled to the output of the ALU to receive the 32-bit result as an output from the ALU;

a memory device communicatively coupled with the second input of the ALU for providing the ALU input-data and communicatively coupled to the output of the ALU for receiving result-data, the memory device comprising a storage location of a size of less than 32 bits;

a sign extender coupled to the memory device for expanding the input-data from the memory to 32-bit data; and

a multiplexer comprising a first and a second input and an output, the first input coupled to the sign extender for receiving the expanded 32-bit data, the second input